

EXHIBIT A

A Complete Set Of The Pending Claims, As Defined By The Previous
Supplemental Amendments And The Amendments Submitted Herewith

1 151. A synchronous memory device including an array of memory
2 cells, the synchronous memory device comprises:

3 clock receiver circuitry to receive an external clock signal;

4 input receiver circuitry to sample a first operation code in
5 response to a rising edge transition of the external clock signal;

6 a programmable register to store a value which is
7 representative of an amount of time to transpire before the memory
8 device outputs data, wherein the memory device stores the value in
9 the programmable register in response to the first operation code;

10 and

11 output driver circuitry to output data in response to a second
12 operation code, wherein the data is output after the amount of time
13 transpires, and wherein:

14 the output driver circuitry outputs a first portion of
15 the data synchronously with respect to a rising edge
16 transition of the external clock signal and outputs a second
17 portion of the data synchronously with respect to a falling
18 edge transition of the external clock signal.

1 152. The memory device of claim 151 wherein the first
2 operation code is included in a control register access packet.

1 153. The memory device of claim 152 wherein the first
2 operation code and the value are included in the same control
3 register access packet.

1 154. The memory device of claim 151 wherein the memory device
2 is a synchronous dynamic random access memory.

1 155. The memory device of claim 151 wherein the input receiver
2 circuitry receives the second operation code and address
3 information.

1 156. The memory device of claim 155 wherein the input receiver
2 circuitry receives the second operation code and the address
3 information on consecutive clock cycles of the external clock
4 signal.

1 157. The memory device of claim 151 wherein the amount of time
2 is a number of clock cycles of the external clock signal.

1 158. The memory device of claim 151 wherein the input receiver
2 circuitry receives a third operation code, wherein the third
3 operation code initiates a write operation in the memory device.

1 159. The memory device of claim 158 wherein the input receiver
2 circuitry receives the third operation code and address
3 information.

1 160. The memory device of claim 151 further including delay
2 lock loop circuitry coupled to the clock receiver circuitry to
3 generate a first internal clock signal, wherein the data is output
4 in response to the first internal clock signal.

1 161. The memory device of claim 151 wherein the output driver
2 circuitry outputs the data onto a bus.

1 162. The memory device of claim 161 wherein the bus includes
2 a set of signal lines to carry multiplexed address information,
3 data and control information.

1 163. A method of operation of a synchronous memory device,
2 wherein the memory device includes an array of memory cells and a
3 programmable register, the method of operation of the memory device
4 comprises:

5 sampling a first operation code synchronously with respect to
6 an external clock signal;

7 receiving a binary value which is representative of an amount
8 of time to transpire before the memory device outputs data in
9 response to a second operation code wherein the memory device
10 stores the binary value in the programmable register in response to
11 the first operation code;

12 sampling the second operation code; and

13 outputting the data after the amount of time transpires,
14 wherein a first portion of the data is output synchronously with
15 respect to a first transition of the external clock signal and a
16 second portion of the data is output synchronously with respect to
17 a second transition of the external clock signal.

1 164. The method of claim 163 wherein the second operation code
2 is sampled synchronously with respect to the external clock signal.

1 165. The method of claim 163 wherein the binary value is
2 representative of a number of clock cycles of the external clock
3 signal.

1 166. The method of claim 165 further including:
2 receiving block size information wherein the block size
3 information defines an amount of data to be output in response to
4 the second operation code, wherein the memory device outputs the
5 amount of data after the number of clock cycles of the external
6 clock signal transpire.

1 167. The method of claim 163 further including receiving
2 address information synchronously with respect to the external
3 clock signal.

1 168. The method of claim 163 wherein the address information
2 and the second operation code are included in a read request
3 packet.

1 169. The method of claim 163 further including receiving
2 precharge information.

1 170. The method of claim 169 wherein the precharge information
2 includes a binary bit, wherein, after accessing the data from the
3 array of memory cells, the memory device retains contents of a
4 plurality of sense amplifiers for a subsequent memory operation as
5 a result of a first state of the binary bit.

1 171. The method of claim 163 wherein the first transition of
2 the external clock signal is a rising edge transition and the
3 second transition of the external clock signal is a falling edge
4 transition.

1 172. The method of claim 171 wherein the first and second
2 transitions of the external clock signal are consecutive
3 transitions of the external clock signal.

1 173. The method of claim 163 wherein the first operation code
2 is sampled during an initialization sequence after power is applied
3 to the memory device.

1 174. The method of claim 163 wherein the memory device outputs
2 the data onto an external bus.

1 175. The method of claim 174 wherein the external bus includes
2 a set of signal lines to carry multiplexed address information,
3 data and control information.

1 176. A method of controlling a synchronous memory device by a
2 memory controller, wherein the memory device includes an array of
3 memory cells and a programmable register, the method of controlling
4 the memory device comprises:

5 providing a first operation code to the memory device, wherein
6 the first operation code initiates an access of the programmable
7 register in the memory device in order to store a binary value;

8 providing the binary value to the memory device, wherein the
9 memory device stores the binary value in the programmable register
10 in response to the first operation code;

11 providing a second operation code to the memory device,
12 wherein the second operation code instructs the memory device to
13 accept data that is issued by the memory controller;

14 providing a first portion of the data to the memory device in
15 response to a rising edge transition of the external clock signal;
16 and

17 providing a second portion of the data to the memory device in
18 response to a falling edge transition of the external clock signal.

1 177. The method of claim 176 wherein the binary value is
2 representative of a delay time to transpire before the memory
3 device samples the data, and wherein the first portion of the data
4 is provided to the memory device after the delay time transpires.

1 178. The method of claim 176 wherein the binary value is
2 representative of a number of clock cycles of the external clock
3 signal to transpire before the memory device samples the data, and

4 wherein the first portion of the data is provided to the memory
5 device after the number of clock cycles transpire.

1 179. The method of claim 176 wherein the binary value is
2 representative of a delay time to transpire before the memory
3 device outputs data in response to an operation code which
4 instructs the memory device to output data.

1 180. The method of claim 176 further including:
2 providing block size information to the memory device, wherein
3 the block size information defines an amount of data to be accepted
4 by the memory device in response to the second operation code.

1 181. The method of claim 176 further including providing
2 address information to the memory device.

1 182. The method of claim 181 wherein the address information
2 and the second operation code are included in a write request
3 packet.

1 183. The method of claim 176 wherein the first operation code
2 and the data are provided to the memory device via an external bus.

1 184. The method of claim 183 wherein the external bus includes
2 a set of signal lines used to carry multiplexed address
3 information, the data and control information.

1 185. The method of claim 176 wherein the second operation code
2 includes precharge information.

1 186. A synchronous memory device, wherein the memory device
2 includes an array of memory cells, the memory device comprises:
3 input receiver circuitry to sample a first operation code in
4 response to a first transition of an external clock signal;
5 a programmable register to store a binary value in response to
6 the first operation code, wherein the binary value is
7 representative of an amount of time to transpire before the memory
8 device outputs data; and
9 output driver circuitry to output data in response to a second
10 operation code and after the amount of time transpires, wherein a
11 first portion of the data is output in response to a second
12 transition of the external clock signal and a second portion of the
13 data is output in response to a third transition of the external
14 clock signal.

1 187. The memory device of claim 186 wherein the binary value
2 is representative of a number of clock cycles of the external clock
3 signal.

1 188. The memory device of claim 186 wherein the second
2 transition of the external clock signal is a rising edge transition
3 and the third transition of the external clock signal is a falling
4 edge transition.

1 189. The memory device of claim 188 wherein the second and
2 third transitions of the external clock signal are consecutive
3 transitions.

1 190. The memory device of claim 189 wherein the first
2 operation code and the binary value are included in a packet.

1 191. The memory device of claim 190 wherein the first
2 operation code and the binary value are included in the same
3 packet.

1 192. The memory device of claim 186 further including delay
2 lock loop circuitry to generate a first internal clock signal,
3 wherein the data is output in response to the first internal clock
4 signal.

1 193. The memory device of claim 186 wherein the input receiver
2 circuitry receives address information.

1 194. The memory device of claim 186 wherein the output driver
2 circuitry outputs the data onto an external bus having a set of
3 signal lines used to carry multiplexed address information, the
4 data and control information.

1 195. The memory device of claim 194 wherein the input receiver
2 circuitry samples the first operation code from the external bus.

1 196. The memory device of claim 186 wherein the output driver
2 circuitry and the input receiver circuitry are connected to a
3 common pad.

1 197. The memory device of claim 186 wherein the memory device
2 is a synchronous dynamic random access memory.

1 198. A synchronous memory device including an array of memory
2 cells, wherein the memory device comprises:

3 a programmable register to store a binary value;

4 a plurality of input receivers to sample first and second
5 operation codes synchronously with respect to an external clock
6 signal, wherein:

7 the first operation code initiates storage of the binary
8 value in the programmable register; and

9 the second operation code initiates a read operation; and

10 a plurality of output drivers to output data in response to
11 the second operation code, wherein:

12 a first portion of the data is output synchronously with
13 respect to a rising edge transition of the external clock
14 signal; and

15 a second portion of the data is output synchronously with
16 respect to a falling edge transition of the external clock
17 signal.

1 199. The memory device of claim 198 wherein the first
2 operation code is sampled synchronously with respect to a first
3 transition of the external clock signal and the second operation
4 code is sampled synchronously with respect to a second transition
5 of the external clock signal.

1 200. The memory device of claim 199 wherein the first
2 operation code is included in a control register access packet and
3 the second operation code is included in a read request packet.

1 201. The memory device of claim 200 wherein the read request
2 packet includes address information.

1 202. The memory device of claim 198 wherein the array of
2 memory cells includes dynamic memory cells.

1 203. The memory device of claim 202 wherein the memory device
2 further includes a delay lock loop, coupled to the plurality of
3 output drivers, to synchronize the outputting of data with the
4 external clock signal.

1 204. The memory device of claim 203 wherein the delay lock
2 loop further includes:

3 a delay line to generate an internal clock signal, wherein the
4 internal clock signal has a delay with respect to the external
5 clock signal; and

6 a comparator to compare the internal clock signal with the
7 external clock signal, wherein the delay of the internal clock
8 signal is adjusted based on the comparison between the internal
9 clock signal and the external clock signal.

1 205. The memory device of claim 198 wherein the second
2 operation code includes precharge information.

1 206. The memory device of claim 205 further including a
2 plurality of sense amplifiers to access the data from the array of
3 memory cells, wherein the precharge information initiates automatic
4 precharge of the plurality of sense amplifiers after the data is
5 accessed from the array of memory cells.

1 207. The memory device of claim 198 wherein the binary value
2 represents a device identifier.

1 208. The memory device of claim 198 wherein the binary value
2 represents a location of a defective portion of the array of memory
3 cells.

1 209. The memory device of claim 198 wherein the binary value
2 represents a delay time.

1 210. The memory device of claim 198 wherein the first portion
2 of data is output, in response to the second operation code, after
3 the delay time transpires.